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1. **Compact thermal models of packages used in conduction cooled applications**
Aranyosi, A.; Ortega, A.; Griffin, R.A.; West, S.; Edwards, D.R.;
Components and Packaging Technologies, IEEE Transactions on [see also Components, Packagir
Technology, Part A: Packaging Technologies, IEEE Transactions on]
Volume 23, Issue 3, Sept. 2000 Page(s):470 - 480
Digital Object Identifier 10.1109/6144.868846
AbstractPlus | References | Full Text: PDF(388 KB) IEEE JNL

2. **A charge pumping device with a potential barrier using inversion charge transfer**
In-Young Chung; Young June Park; Hong Shick Min;
Electron Devices, IEEE Transactions on
Volume 48, Issue 6, June 2001 Page(s):1216 - 1221
Digital Object Identifier 10.1109/16.925250
AbstractPlus | References | Full Text: PDF(128 KB) IEEE JNL

3. **Altering transistor positions: Impact on the performance and power dissipation of dynamic l**
Mishra, S.M.; Rofail, S.S.; Seng, Y.K.;
Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G- Circuits, Devices ai
Volume 146, Issue 5, Oct. 1999 Page(s):279 - 284
Digital Object Identifier 10.1049/ip-cds:19990580
AbstractPlus | Full Text: PDF(352 KB) IEE JNL

4. **Design of a floating node voltage-controlled linear variable resistor circuit**
Kushima, M.; Inaba, M.; Tanno, K.; Ishizuka, O.;
Circuits and Systems, 2004. MWSCAS '04. The 2004 47th Midwest Symposium on
Volume 1, 25-28 July 2004 Page(s):I - 85-8 vol.1
Digital Object Identifier 10.1109/MWSCAS.2004.1353903
AbstractPlus | Full Text: PDF(357 KB) IEEE CNF

5. **Comparison of quasi-/pseudo-floating gate techniques**
Inchang Seo; Fox, R.M.;
Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on
Volume 1, 23-26 May 2004 Page(s):I-365 - I-368 Vol.1
AbstractPlus | Full Text: PDF(345 KB) IEEE CNF

6. **Systematic memory test generation for DRAM defects causing two floating nodes**
Al-Ars, Z.; van de Goor, Ad.J.;

Memory Technology, Design and Testing, 2003. Records of the 2003 International Workshop on
28-29 July 2003 Page(s):27 - 32

AbstractPlus | Full Text: PDF(322 KB) IEEE CNF

7. **Random pattern testability of the open defect detection method using application of time-va**
Yotsuyanagi, H.; Hashizume, M.; Iwakiri, T.; Ichimiya, M.; Tamesada, T.;
Electronic Design, Test and Applications, 2002. Proceedings. The First IEEE International Worksh
29-31 Jan. 2002 Page(s):387 - 391
Digital Object Identifier 10.1109/DELTA.2002.994656

AbstractPlus | Full Text: PDF(292 KB) IEEE CNF

8. **Test pattern for supply current test of open defects by applying time-variable electric field**
Yotsuyanagi, H.; Hashizume, M.; Iwakiri, T.; Ichimiya, M.; Tamesada, T.;
Defect and Fault Tolerance in VLSI Systems, 2001. Proceedings. 2001 IEEE International Sympos
24-26 Oct. 2001 Page(s):287 - 295
Digital Object Identifier 10.1109/DFTVS.2001.966781

AbstractPlus | Full Text: PDF(173 KB) IEEE CNF

9. **An SOI single-electron transistor**
Xiaohui Tang; Baie, X.; Bayot, V.; Van de Wiele, F.; Colinge, J.P.;
SOI Conference, 1999. Proceedings. 1999 IEEE International
4-7 Oct. 1999 Page(s):46 - 47
Digital Object Identifier 10.1109/SOI.1999.819851

AbstractPlus | Full Text: PDF(96 KB) IEEE CNF

10. **An SOI nano flash memory device**
Xiaohui Tang; Baie, X.; Bayot, V.; Van de Wiele, F.; Colinge, J.P.;
SOI Conference, 1999. Proceedings. 1999 IEEE International
4-7 Oct. 1999 Page(s):100 - 101
Digital Object Identifier 10.1109/SOI.1999.819872

AbstractPlus | Full Text: PDF(100 KB) IEEE CNF

11. **Compact thermal models of conduction cooled packages**
Ortega, A.; Aranyosi, A.; Griffin, R.A.; West, S.; Edwards, D.;
Semiconductor Thermal Measurement and Management Symposium, 1999. Fifteenth Annual IEEE
9-11 March 1999 Page(s):221 - 230
Digital Object Identifier 10.1109/STHERM.1999.762452

AbstractPlus | Full Text: PDF(708 KB) IEEE CNF

12. **Detecting resistive shorts for CMOS domino circuits**
Chang, J.T.-Y.; McCluskey, E.J.;
Test Conference, 1998. Proceedings. International
18-23 Oct. 1998 Page(s):890 - 899
Digital Object Identifier 10.1109/TEST.1998.743280

AbstractPlus | Full Text: PDF(1004 KB) IEEE CNF

13. **Stability of highpass and bandreject analog continuous-time OTA-C filters**
Galvez-Durand, F.; Caloba, L.; de Queiroz, A.C.M.;
Circuits and Systems, 1997. Proceedings of the 40th Midwest Symposium on
Volume 1, 3-6 Aug. 1997 Page(s):64 - 67 vol.1
Digital Object Identifier 10.1109/MWSCAS.1997.666034

AbstractPlus | Full Text: PDF(348 KB) IEEE CNF

14. **Burn-in problem on 0.5 μm 1 MB SRAM-the role of barrier glue layer on the W plug**
Chan, C.M.; Hisham, N.; Soon, F.Y.; Tatti, S.; Widener, E.;
Semiconductor Electronics, 1996. ICSE '96. Proceedings., 1996 IEEE International Conference on
26-28 Nov. 1996 Page(s):89 - 92
Digital Object Identifier 10.1109/SMELEC.1996.616459

AbstractPlus | Full Text: PDF(420 KB) IEEE CNF

15. **Asymptotic waveform evaluation for circuits containing floating nodes**
Pillage, L.T.; Huang, X.; Rohrer, R.A.;
Circuits and Systems, 1990., IEEE International Symposium on
1-3 May 1990 Page(s):613 - 616 vol.1
Digital Object Identifier 10.1109/ISCAS.1990.112137
AbstractPlus | Full Text: PDF(248 KB) IEEE CNF

16. **Differential cascode voltage switch with the pass-gate (DCVSPG) logic tree for high perform systems**
Lai, F.S.; Hwang, W.;
VLSI Technology, Systems, and Applications, 1993. Proceedings of Technical Papers. 1993 Intern
12-14 May 1993 Page(s):358 - 362
Digital Object Identifier 10.1109/VTSA.1993.263680
AbstractPlus | Full Text: PDF(288 KB) IEEE CNF

17. **Wafer level detecting of Idd failures in CMOS ASICs using liquid crystal techniques**
Ma, J.; Haley, M.W.; Mitchell, T.W.; Sanchez, I.;
University/Government/Industry Microelectronics Symposium, 1993., Proceedings of the Tenth Bie
18-19 May 1993 Page(s):240 - 244
Digital Object Identifier 10.1109/UGIM.1993.297060
AbstractPlus | Full Text: PDF(924 KB) IEEE CNF

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Circuits and Systems, 2004. MWSCAS '04. The 2004 47th Midwest Symposium on
Volume 1, 25-28 July 2004 Page(s):I - 85-8 vol.1
Digital Object Identifier 10.1109/MWSCAS.2004.1353903
AbstractPlus | Full Text: PDF(357 KB) IEEE CNF

2. **Asymptotic waveform evaluation for circuits containing floating nodes**
Pillage, L.T.; Huang, X.; Rohrer, R.A.;
Circuits and Systems, 1990., IEEE International Symposium on
1-3 May 1990 Page(s):613 - 616 vol.1
Digital Object Identifier 10.1109/ISCAS.1990.112137
AbstractPlus | Full Text: PDF(248 KB) IEEE CNF

3. **A continuously-adapting analog node using floating-gate synapses**
Dugger, J.; Hasler, P.;
Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium on
Volume 3, 8-11 Aug. 2000 Page(s):1058 - 1061 vol.3
Digital Object Identifier 10.1109/MWSCAS.2000.951398
AbstractPlus | Full Text: PDF(312 KB) IEEE CNF

4. **Floating-point bitwidth analysis via automatic differentiation**
Gaffar, A.A.; Mencer, O.; Luk, W.; Cheung, P.Y.K.; Shirazi, N.;
Field-Programmable Technology, 2002. (FPT). Proceedings. 2002 IEEE International Conference c
16-18 Dec. 2002 Page(s):158 - 165
AbstractPlus | Full Text: PDF(415 KB) IEEE CNF

5. **Numerical observability analysis based on network graph theory**
Korres, G.N.; Katsikas, P.J.; Clements, K.A.; Davis, P.W.;
Power Systems, IEEE Transactions on
Volume 18, Issue 3, Aug. 2003 Page(s):1035 - 1045
Digital Object Identifier 10.1109/TPWRS.2003.814882
AbstractPlus | References | Full Text: PDF(507 KB) IEEE JNL

6. **Development of compact thermal models for advanced electronic packaging: methodology : validation for a single-chip CPGA package**
Aranyosi, A.; Ortega, A.; Evans, J.; Tarter, T.; Pursel, J.; Radhakrishnan, J.;

Thermal and Thermomechanical Phenomena in Electronic Systems, 2000. ITHERM 2000. The Se
Conference on
Volume 1, 23-26 May 2000 Page(s):
Digital Object Identifier 10.1109/ITHERM.2000.866829

AbstractPlus | Full Text: PDF(828 KB) IEEE CNF

7. **Weight-free relaxation**
Le, N.T.; Vidal, J.J.;
Neural Networks, 1989. IJCNN., International Joint Conference on
18-22 June 1989 Page(s):581 vol.2
Digital Object Identifier 10.1109/IJCNN.1989.118337

AbstractPlus | Full Text: PDF(92 KB) IEEE CNF